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22 SEP 95 11:57:32 U.S. Patent & Trademark Office P0002
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FILE 'USPAT' ENTERED AT 11:57:32 ON 22 SEP 95

* * * * *
* WELCOME TO THE *
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* * * * *

=> s (semiconductor(w)chip#) (p)encapsulat?
113433 SEMICONDUCTOR
95733 CHIP#
44036 ENCAPSULAT?
L1 575 (SEMICONDUCTOR(W)CHIP#) (P)ENCAPSULAT?

=> s l1 and ring#
434840 RING#
L2 83 L1 AND RING#

=> d 1-30

1. 5,441,902, Aug. 15, 1995, Method for making channel stop structure for CMOS devices; ' Shio-Ming Hsieh; et al., 437/34; 257/369; 437/57, 69, 70 [IMAGE AVAILABLE]
2. 5,408,741, Apr. 25, 1995, Method for forming electronic device; Jon M. Long, 29/827; 174/52.2; 437/206, 207, 208 [IMAGE AVAILABLE]
3. 5,397,528, Mar. 14, 1995, Method of closing a mould before at least partly filling a cavity of this mould with a solidifiable liquid; Josephus J. M. Schraven, et al., 264/328.1; 425/589 [IMAGE AVAILABLE]
4. 5,395,226, Mar. 7, 1995, Molding machine and method; Kunito Sakai, et al., 425/116; 249/90, 93, 95; 264/272.17; 425/117, DIG.228 [IMAGE AVAILABLE]
5. 5,384,488, Jan. 24, 1995, Configuration and method for positioning semiconductor device bond pads using additional process layers; Shahin Golshan, et al., 257/786, 692 [IMAGE AVAILABLE]
6. 5,346,743, Sep. 13, 1994, Resin encapsulation type semiconductor device; 11:59:42 COPY AND CLEAR PAGE, PLEASE

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- 22 SEP 95 12:00:07 U.S. Patent & Trademark Office P0003
 Ken Uchida, et al., 428/76; 174/52.2; 257/789, 793 [IMAGE AVAILABLE]
7. 5,336,752, Aug. 9, 1994, Method for producing phenolic resin; Fumiaki Oshimi, et al., 528/205, 212, 214; 568/718, 719, 721, 749 [IMAGE AVAILABLE]
8. 5,311,060, May 10, 1994, Heat sink for semiconductor device assembly; Michael D. Rostoker, et al., 257/796, 667, 675, 676, 713; 361/714 [IMAGE AVAILABLE]
9. 5,308,797, May 3, 1994, Leads for semiconductor chip assembly and method; David R. Kee, 437/209; 257/666, 695; 437/206, 211, 217, 220 [IMAGE AVAILABLE]
10. 5,304,847, Apr. 19, 1994, Direct thermocompression bonding for thin electronic power chips; Constantine A. Neugebauer, et al., 257/762, 677, 765, 766, 785; 361/813 [IMAGE AVAILABLE]
11. 5,304,512, Apr. 19, 1994, Process for manufacturing semiconductor integrated circuit device, and molding apparatus and molding material for the process; Katsuo Arai, et al., 437/211; 264/272.11, 272.14, 272.17; 437/209, 212, 214, 216, 217, 219 [IMAGE AVAILABLE]
12. 5,294,835, Mar. 15, 1994, Epoxy resin composition for semiconductor encapsulation and semiconductor device using the same; Kazumasa Igarashi, et al., 257/793, 788; 528/406 [IMAGE AVAILABLE]
13. 5,292,688, Mar. 8, 1994, Solder interconnection structure on organic substrates and process for making; Richard Hsiao, et al., 437/209, 211, 212, 213 [IMAGE AVAILABLE]
14. 5,276,354, Jan. 4, 1994, Integrated circuit package with battery housing; Joseph Link, et al., 307/66; 257/666, 678, 724; 307/150 [IMAGE AVAILABLE]
15. 5,275,841, Jan. 4, 1994, Method for encapsulating integrated circuit; Ching-Ping Wong, 427/96, 400 [IMAGE AVAILABLE]
16. 5,270,262, Dec. 14, 1993, 0-ring package; Andrew P. Switky, et al., 437/217, 209, 215, 220, 221 [IMAGE AVAILABLE]
17. 5,255,157, Oct. 19, 1993, Plastic pin grid array package with locking pillars; Uli Hegel, 361/783; 174/52.2; 257/787; 361/761, 807 [IMAGE AVAILABLE]
18. 5,252,053, Oct. 12, 1993, Apparatus for closing a mold; Josephus J. M. Schraven, et al., 382/233; 100/258R, 270; 264/272.11; 425/129.1, 150, 406, 451.2, 451.9 [IMAGE AVAILABLE]
19. 5,251,168, Oct. 5, 1993, Boundary cells for improving retention time in memory devices; Gishi Chung, et al., 365/51, 63, 149, 189.09, 230.03 [IMAGE AVAILABLE]
20. 5,250,848, Oct. 5, 1993, Solder interconnection structure; Frederick R. Christie, et al., 257/778; 228/180.1, 180.22; 257/687, 786, 793; 361/765; 428/411.1, 422.8; 525/107, 122; 528/210, 211, 422 [IMAGE AVAILABLE]
21. 5,227,663, Jul. 13, 1993, Integral dam and heat sink for semiconductor device assembly; Sadanand Patil, et al., 257/718, 688, 705, 706, 719, 796; 361/717 [IMAGE AVAILABLE]

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22 SEP 95 12:02:11 U.S. Patent & Trademark Office P0004
 22. 5,210,375, May 11, 1993, Electronic device package--carrier assembly ready to be mounted onto a substrate; Jon M. Long, 174/52.4, 52.2; 257/787 [IMAGE AVAILABLE]

23. 5,206,186, Apr. 27, 1993, Method for forming semiconductor electrical contacts using metal foil and thermocompression bonding; Constantine A. Neugebauer, et al., 437/183; 228/254; 257/133; 437/190, 192, 194, 197 [IMAGE AVAILABLE]

24. 5,194,930, Mar. 16, 1993, Dielectric composition and solder interconnection structure for its use; Kostas Papathomas, et al., 257/773, 779 [IMAGE AVAILABLE]

25. 5,185,653, Feb. 9, 1993, 0-~~ring~~ package; Andrew P. Switky, et al., 257/729; 72/70; 257/666, 789 [IMAGE AVAILABLE]

26. 5,184,206, Feb. 2, 1993, Direct thermocompression bonding for thin electronic power chips; Constantine A. Neugebauer, et al., 257/762, 765, 766 [IMAGE AVAILABLE]

27. 5,182,424, Jan. 26, 1993, Module encapsulation by induction heating; Vlastimil Frank, 219/604; 174/52.2, 52.4; 219/633, 651; 257/697; 437/180, 219 [IMAGE AVAILABLE]

28. 5,175,612, Dec. 29, 1992, Heat sink for semiconductor device assembly; Jon Long, et al., 257/667, 668, 675, 676; 361/714 [IMAGE AVAILABLE]

29. 5,168,368, Dec. 1, 1992, Lead frame-chip package with improved configuration; John Gow, 3rd, et al., 257/666, 668, 670, 784 [IMAGE AVAILABLE]

30. 5,165,956, Nov. 24, 1992, Method of encapsulating an electronic device with a silicone encapsulant; Ching-Ping Wong, 427/96, 387, 407.1 [IMAGE AVAILABLE]

=> s l1 and solder(w)mask#) (p) (epoxy(w) (acrylic or acrylate#))
 UNMATCHED RIGHT PARENTHESIS 'MASK#)' (P'

=> s l1 and (solder(w)mask#) (p) (epoxy(w) (acrylic or acrylate#))

28496 SOLDER

68422 MASK#

89806 EPOXY

88442 ACRYLIC

58446 ACRYLATE#

9 (SOLDER(W)MASK#) (P) (EPOXY(W) (ACRYLIC OR ACRYLATE#))

L3 0 L1 AND (SOLDER(W)MASK#) (P) (EPOXY(W) (ACRYLIC OR ACRYLATE#))

=> s l1 and (barrier# or film# or coat?) (p) (epoxy(w) (acrylic# or acrylate#))

84143 BARRIER#

283474 FILM#

361546 COAT?

89806 EPOXY

90780 ACRYLIC#

58446 ACRYLATE#

597 (BARRIER# OR FILM# OR COAT?) (P) (EPOXY(W) (ACRYLIC# OR ACRYLATE#))

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22 SEP 95 12:12:26 U.S. Patent & Trademark Office P0005
 L4 0 L1 AND (BARRIER# OR FILM# OR COAT?) (P) (EPOXY(W) (ACRYLIC# OR AC
 RYLATE#))

=> s l1 and (solder(w)mask#) (p) (epoxy(w)acrylic#)

28496 SOLDER

68422 MASK#

89806 EPOXY

90780 ACRYLIC#

1 (SOLDER(W)MASK#) (P) (EPOXY(W)ACRYLIC#)

L5 0 L1 AND (SOLDER(W)MASK#) (P) (EPOXY(W)ACRYLIC#)

=> s l1 and (solder(w)mask#) (p) ((vacuum or vacuo) (12a) laminat?)

28496 SOLDER

68422 MASK#

251148 VACUUM

42968 VACUO

93141 LAMINAT?

38 (SOLDER(W)MASK#) (P) ((VACUUM OR VACUO) (12A) LAMINAT?)

L6 0 L1 AND (SOLDER(W)MASK#) (P) ((VACUUM OR VACUO) (12A) LAMINAT?)

=> s l1 and (barrier# or film# or coat?) (p) ((vacuum or vacuo) (12a) laminat?)

84143 BARRIER#

283474 FILM#

361546 COAT?

251148 VACUUM

42968 VACUO

93141 LAMINAT?

1280 (BARRIER# OR FILM# OR COAT?) (P) ((VACUUM OR VACUO) (12A) LAM
)

L7 3 L1 AND (BARRIER# OR FILM# OR COAT?) (P) ((VACUUM OR VACUO) (12A) L
 AMINAT?)

=> d 1-3

1. 4,918,811, Apr. 24, 1990, Multichip integrated circuit packaging method;
 Charles W. Eichelberger, et al., 29/840; 437/209 [IMAGE AVAILABLE]

2. 4,783,695, Nov. 8, 1988, Multichip integrated circuit packaging
 configuration and method; Charles W. Eichelberger, et al., 257/668, 700, 723
 [IMAGE AVAILABLE]

3. 4,063,229, Dec. 13, 1977, Article surveillance; John Welsh, et al.,
 340/571; 206/807; 219/664 [IMAGE AVAILABLE]

=> s (solder(w)mask#) (p) (epoxy(w)acrylic#)

28496 SOLDER

68422 MASK#

89806 EPOXY

90780 ACRYLIC#

L8 1 (SOLDER(W)MASK#) (P) (EPOXY(W)ACRYLIC#)

=> d

1. 5,304,252, Apr. 19, 1994, Method of removing a permanent photoimagable
 12:24:48 COPY AND CLEAR PAGE, PLEASE

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22 SEP 95 12:25:12 U.S. Patent & Trademark Office P0006
film from a printed circuit board; Richard C. Condra, et al., 134/2, 29, 38;
430/329, 330, 331 [IMAGE AVAILABLE]

=> d his

(FILE 'USPAT' ENTERED AT 11:57:32 ON 22 SEP 95)

SET PAGELNGTH 62

SET LINELENGTH 78

L1 575 S (SEMICONDUCTOR(W)CHIP#) (P)ENCAPSULAT?
L2 83 S L1 AND RING#
L3 0 S L1 AND (SOLDER(W)MASK#) (P) (EPOXY(W) (ACRYLIC OR ACRYLATE#))
L4 0 S L1 AND (BARRIER# OR FILM# OR COAT?) (P) (EPOXY(W) (ACRYLIC# OR
L5 0 S L1 AND (SOLDER(W)MASK#) (P) (EPOXY(W)ACRYLIC#)
L6 0 S L1 AND (SOLDER(W)MASK#) (P) ((VACUUM OR VACUO) (12A)LAMINAT?)
L7 3 S L1 AND (BARRIER# OR FILM# OR COAT?) (P) ((VACUUM OR VACUO) (12
L8 1 S (SOLDER(W)MASK#) (P) (EPOXY(W)ACRYLIC#)

=>

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